INTEGRATED CIRCUIT AND METHOD OF PRODUCING A CARRIER WAFER FOR AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuits, and in particular, to a method of producing a carrier wafer for an integrated circuit.

BACKGROUND OF THE INVENTION

[0002] In manufacturing semiconductor devices, it is imperative that the devices are defect free at the time of production, and reliable throughout their use. When defects are found in completed devices, the percentage of usable devices increases, and the profitability of the manufacturer suffers. More importantly, when a semiconductor device fails after been installed a device, such a failure can cause the entire device to fail. That is, the failure of a single semiconductor device can render an entire consumer electronics device unusable. Accordingly, it is important that manufacturers of semiconductor devices minimize defects whenever possible.

[0003] One area where defects can occur as in the area of wire bonding. Wire bonds are used to connect a bond pad on one element of a device, such as a carrier wafer, to a bond pad on another element, such as a substrate receiving carrier wafer. Two types of wire bonding which are commonly used include ball bonding and wedge bonding. Gold-ball bonding is the most popular method. In this process, a melted sphere of gold bonds a length of wire down as a first bond. A loop drawn out from the first bond then connects the wire, and then reforms another ball for the subsequent ball bond. Gold-wire bonding is characterized as a thermosonic process, meaning that heat, ultrasonics, force, and time are all used to effect the bond. A second method of wire bonding is the

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wedge bonding process. This process is primarily used with aluminum wire but also can be used with gold wire. Usually performed at an ambient temperature, wedge bonding involves putting two wedge bonds down. No ball is formed in this process. This aluminum bond process is characterized as an ultrasonic wire bond, meaning only ultrasonic energy, force, and time are used to create the bond.

[0004] The use of these types of processes depends on the specific type of application. For example, gold-wire bonding is used in most high volume applications because it is a faster process. Aluminum-wire bonding is used in situations when packages or a PCB cannot be heated. In addition, the wedge bonding process can attain a finer pitch than gold-wire bonding. Gold-wire bonding, for example, requires smooth, clean bond surfaces. Typically, gold wire is bonded to an aluminum pad on the die and thick-or thin-film gold metallization on the substrate. The cleanliness of the substrate affects the reliability of the bond. Although organic contamination can be removed with a cleaning process, such as argon plasma cleaning, such removal requires additional time and expense.

[0005] When producing a carrier wafer having bond pads, a number of processing steps are performed before a wire bond is ever attached to the bond pad of the wafer carrier. In some instances, for example when a flip chip is attached to the carrier wafer, a bump pad on a carrier wafer for receiving a solder bump is formed at the same time that a wire bond pad is formed. While various steps for enabling a flip chip to be attached to the carrier wafer are performed on the bond pad, such as the application of an under bump metallization layer and the solder bump itself, the wire bond pad on the carrier wafer remains exposed. That is, the surface of the wire bond pad is often exposed to processing steps for other areas of the carrier wafer. Accordingly, the

wire bond pad can often become contaminated, rendering the wire bond pad difficult to bond.

[0006] Accordingly, there is a need for an improved integrated circuit and method of producing an integrated circuit integrated circuit having improved wire bond pads.

SUMMARY OF THE INVENTION

[0007] A method of producing a carrier wafer for an integrated circuit is disclosed. The method preferably provides a carrier wafer having a plurality of bump pads and a plurality of wire bond pads. A passivation layer is provided on the carrier wafer, and then etched over a portion of the plurality of bump pads. Solder bumps and other metallization layers are then applied on the bump pads. The passivation layer over at least a portion of the plurality of wire bond pads is then separately. By providing the separate etching step, the wire bond pads remain uncontaminated, thereby providing a better surface for a wire bond. A method of assembling a carrier wafer having one or more flip chips and a method of assembling a multi-chip modules are also described

[0008] An integrated circuit employing a carrier wafer is also disclosed. The integrated circuit preferably comprises a carrier wafer having a plurality of bump pads and a plurality of wire bond pads. A passivation layer is also formed on the carrier wafer over the plurality of bump pads and the plurality of wire bond pads. A solder bump is provided on a bump pad within a first etched window formed in a first etching step in the passivation layer. A second etched window is also provided over at least a portion of the wire bond pad. The second etched window is formed in the passivation layer by a second etching step. Accordingly, the wire bond pads remain uncontaminated, and provide a better surface for a wire bond.

[0009] A completed carrier wafer and a fully assembled multi-chip module employing a plurality of flip chips including a carrier wafer processed according to the present invention are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 is a top plan view of a multi-chip module according to an embodiment of the present invention;

[0011] Fig. 2 is a cross sectional view of the multi-chip module of Fig. 1 taken at lines 2-2 according to an embodiment of the present invention;

[0012] Figs. 3A-3H is a series of cross sectional views showing the formation of a carrier wafer according to an embodiment of the present invention;

[0013] Fig. 4A-4G is a series of cross sectional views showing the formation of a multi-chip module according to an embodiment of the present invention;

[0014] Fig. 5 is a flow chart showing a method of forming a carrier wafer according to an embodiment of the present invention;

[0015] Fig. 6 is a flow chart showing a method of assembling a carrier wafer according to an embodiment of the present invention; and

[0016] Fig. 7 is a flow chart showing a method of assembling a multi-chip module according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0017] Turning first to Figs. 1 and 2, a multi-chip module according to an embodiment of the present invention is shown. In particular, integrated circuit 100 comprises a substrate 102 having a plurality of wire bond pads 103. A carrier wafer 104 is coupled to the integrated circuit 100, as is shown in more detail in reference to the cross-section of figure 2. A plurality of flip chips 106 are positioned on

the carrier wafer 104. The carrier wafer 104 could be for example, a silicon carrier wafer, or some other suitable material. Bump pads 202 on the carrier wafer enable coupling the flip chips 106 to the substrate 102. The substrate 102 could be a ceramic substrate, or some other organic substrate. Solder bumps 204 enable a connection to contact pads 206. Finally, lines 210 generally enable the coupling of the two or more flip chips, and in particular, the coupling of regions of the flip chip employing programmable logic. Such coupling of programmable logic in flip chips is described in more detail in US Application Serial No. 10/624,832 Entitled "A Programmable Multi-Chip Module," filed on July 21, 2003 and assigned to the assignee of the present invention, the entire application of which is incorporated herein by reference.

[0018] Turning now to Figs. 3A-3H, a series of cross sectional views shows the formation of a carrier wafer according to an embodiment of the present invention. The carrier wafer 104 comprises a plurality of wire bond pads 108 and a plurality of bump pads 202 as shown in Fig. 3-A. The carrier wafer can be a silicon die, for example, or some other suitable material. The bump pads and the wire bond pads are preferably formed by a metallization process, but could be formed by another suitable process, such as diffusion techniques. The carrier wafer preferably has interconnecting traces, such as lines 210 of Fig. 2, also formed by metallization or some other technique, and may include passive elements, such as resistors, inductors or capacitors.

[0019] A passivation layer 302 is then applied, as shown in Fig. 3-B. The passivation layer is then etched to form an etched window exposing the bump pad 202, as shown in Fig. 3-C. However, it should be noted that the wire bond pad 108 remains unetched. Accordingly, the wire bond pads remain clean during remaining steps of the semiconductor

manufacturing process, such as the application of an under bump metallization (UBM) layer and a solder bump.

[0020] A dielectric layer 306 is then applied over the passivation layer 302, as shown in Fig. 3-D. The dielectric layer 306 is then etched to again expose bump pad 202 through etched window 308 and create an etched window 310. The passivation layer 306 still remains over the wire bond pad 302, as shown in Fig. 3-E. Metallization steps can then be performed without contaminating the wire bond pad 108. In particular, an under bump metallization layer 312 can be applied as shown in Fig. 3-F, while a solder bump 314 can be applied as shown in Fig. 3-G. However, no materials from the metallization steps can be deposited on the wire bond pad 108.

[0021] Photoresist is then applied over the carrier wafer and the windows are etched for the intended wire bond areas. A dry or wet etch process can then be used to remove the passivation over the wire bond pads, as shown in Fig. 3-H. After the wire bond openings are formed, the resist is stripped off using either a wet or dry etching process leaving opening 316. The silicon wafer is then sent for further flip chip assembly processing as shown in Fig. 4.

[0022] Turning now to Fig. 4A-4G, a series of cross sectional views shows the formation of a multi-chip module according to an embodiment of the present invention. In particular, a plurality of flip chips 106 is attached to a carrier wafer 104 as shown in Fig. 4A. An underfill layer 401 is then applied as shown in Fig. 4B. The carrier wafer 104 is then coupled to a substrate 102 as shown in Fig. 4C. Wire bonds 402 are then made between the wire bond pads 108 of the carrier wafer 104 and the wire bond pads 103 of the substrate 102, as shown in Fig. 4D. An encapsulation layer 404 is then applied over the flip chips 106 and the wire bonds 402 as shown in Fig. 4E. In addition to providing protection for the wire bonds, the encapsulation layer can

also provide heat conductive qualities to improve the heat dissipation in the device. Solder balls 406 are then applied to the bottom of the substrate as shown in Fig. 4F. The solder bumps 406 enable the attachment of the multi-chip module to a circuit board for use in a device, such as a consumer electronics device. Finally, a metal lid 408 or some other suitable cover is applied over the substrate to enclose the encapsulation layer and the wire bonds, as shown in Fig. 4-G.

[0023] Turning now to Fig. 5, a flow chart shows a method of forming a carrier wafer according to an embodiment of the present invention. The method preferably comprises a step of providing a carrier wafer having a plurality of bump pads and a plurality of wire bond pads at a step 502. A suitable carrier wafer could be a silicon carrier wafer. A passivation layer is then applied to the carrier wafer at a step 504. The passivation layer over at least a portion of the plurality of bump pads is then etched at a step 506. It should be noted however that the passivation layer is not etched over wire bond pads of the carrier wafer. Solder bumps and any other metallization, such as an under bump metallization, are then applied on the plurality of bump pads at a step 508. Finally, the passivation layer over at least a portion of the plurality of wire bond pads is then separately etched over the wire bond pads at a step 510. Because the etching step of the wire bond pads is performed after the metallization or other processing steps, the wire bond pads are not contaminated, thereby improving the quality of the wire bond between the wire bond pad and some other contact, such as a wire bond pad on a substrate.

[0024] Turning now to Fig. 6, a flow chart shows a method of assembling a carrier wafer according to an embodiment of the present invention. The method enables employing a flip chip in an integrated circuit, and preferably comprises a step of providing a passivation layer over a plurality of

bump pads and a plurality of wire bond pads formed on a carrier wafer at a step 602. The passivation layer over at least a portion of the plurality of bump pads is then etched at a step 604. Solder bumps and any underbump metallization are the applied on the plurality of bump pads at a step 606. The passivation layer over at least a portion of the plurality of the wire bond pads is then separately etched at a step 608. A flip chip is then coupled to the plurality of bump pads at a step 610.

[0025] Turning now to Fig. 7, a flow chart shows a method of assembling a multi-chip module according to an embodiment of the present invention. The method employs a plurality of flip chips in an integrated circuit, and preferably comprises the steps of providing a silicon carrier wafer having a plurality of bump pads connected by a plurality of traces and a plurality of wire bond pads at a step 702. A passivation layer is then provided on the plurality of bump pads and the plurality of wire bond pads at a step 704. The passivation layer over the plurality of bump pads is then etched at step 706. The solder bumps and any other metallization layer are then applied on the plurality of bump pads at a step 708. The passivation layer over the plurality of wire bond pads is then separately etched at a step 710. A plurality of flip chips is then positioned on the plurality of bump pads at a step 712. The flip chips are applied to the carrier wafer at a step 714 and underfill is applied at a step 716. The carrier wafer is then coupled to a substrate at a step 718. A plurality of wire bonds are then provided between the plurality of wire bond pads on the carrier wafer and a plurality of wire bond pads on the substrate at a step 720. An encapsulation layer is applied over the flip chips and the plurality of wire bonds at a step 722. A plurality of solder balls is then applied to the substrate at a step 724. Finally, a metal lid or some other suitable cover is then attached over the substrate at a step 726.

[0026] It can therefore be appreciated that the new and novel integrated circuit and method of employing a flip chip in an integrated circuit has been described. It will be appreciated by those skilled in the art that, particular the teaching herein, numerous alternatives and equivalents will be seen to exist which incorporate the disclosed invention. As a result, the invention is not to be limited by the foregoing embodiments, but only by the following claims.